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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,639	04/06/2005	Carlos Antonio Alba Pinto	NL02 0976 US	7526

24738 7590 04/30/2007
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER

TRAN, VINCENT HUY

ART UNIT	PAPER NUMBER
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2115

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/530,639

Applicant(s)

ALBA PINTO ET AL.

Examiner

Vincent T. Tran

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-9 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 April 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 4/6/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 4/6/05
2. Claims 1-9 are pending for examination.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 4/6/05 were considered by the examiner.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "memory units 12a-g". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Feierbach U.S. Patent No. 7,107,471.

8. As per claim 1, Feierbach discloses data processing apparatus, the apparatus comprising :
an instruction memory system [102 fig. 1; 308 fig. 3] arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses;

an instruction execution unit [1-7-110 fig. 1; 302s fig. 3], comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units [col. 6 lines 23-31];

a power saving circuit [112 fig. 1; 306, 304 fig. 3] arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the

Art Unit: 2115

power saving circuit being arranged to select the functional units and/or parts of the instruction memory in the subset dependent on program execution [col. 4 lines 16-45; col. 6 lines 43-62].

9. As per claim 2, Feierbach discloses clock signals to the functional units and/or parts of the instruction memory in the subset are disabled in said power saving state [col. 2 lines 1-4].

10. As per claim 3, Feierbach discloses the functional units are organized into groups of one or more functional units each, the functional unit or units in each respective group [fig. 6] receiving instructions from a respective instruction field in the instruction word, each time for execution by one of the functional units in the group, the power saving circuit selecting the functional units that are switched to the power saving state per group [col. 2 lines 7-11].

11. Claims 1-4, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Bartley U.S. Patent No. 6,219,796

12. As per claim 1, Bartley discloses data processing apparatus, the apparatus comprising :
an instruction memory system [12, 11a, 11b fig. 1] arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses [col. 3 lines 16-21];

an instruction execution unit [11d, 11e fig. 1], comprising a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units [col. 3 lines 41-61];

a power saving circuit [18 fig. 1] arranged to switch a selectable subset of the functional units and/or parts of the instruction memory that supply instructions from the instruction word to the functional units to a power saving state during program execution, the power saving circuit being arranged to select the functional units and/or parts of the instruction memory in the subset dependent on program execution [col. 6 lines 34-43].

13. As per claim 2, Bartley discloses clock signals to the functional units and/or parts of the instruction memory in the subset are disabled in said power saving state [col. 6 lines 40-43].

14. As per claim 3, Bartley discloses the functional units are organized into groups of one or more functional units each [group 11d and group 11e], the functional unit or units in each respective group receiving instructions from a respective instruction field in the instruction word, each time for execution by one of the functional units in the group, the power saving circuit selecting the functional units that are switched to the power saving state per group [col. 6 lines 36-39].

15. As per claim 4, Bartley discloses the instruction memory system comprises a plurality of memory units [Register File in 11d and 11e or 12], each for supplying a respective instruction field in the instruction word for an instruction work for an instruction for a respective functional unit or group of functional units, the clock gating circuit being arranged to switch those memory units to the power saving state that supply the instruction field that for the selectable ones of the functional units that are switched to the power saving state [col. 6 lines 36-47].

16. As per claim 6, Bartley inherently teaches the power saving circuit is arranged to select the subset dependent an instruction address associated with instruction word [col. 6 lines 42-43 – portion of memory could similarly powered down].

17. As per claim 7, Barley discloses the powering saving circuit is arranged to select the subset under control of one or more instructions contained in a program executed by the data processing apparatus [col. 5 lines 55-66].

18. As per claim 8, Barley discloses one or more instructions specify the subset [col. 6 lines 1-3].

19. As per claim 9, Barley discloses identifying a part of the program wherein the instruction word does not contain instructions for functional units in a particular one of the groups, and using the powering saving circuit to switch to the power saving state the functional units that not contained in the particular one of the group and/or memory units that are coupled to the particular one of the groups, during executing of said identified part of the program [col. 6 lines 25-32].

Allowable Subject Matter

20. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

Art Unit: 2115

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (571)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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